

# IRFW644B / IRFI644B

## 250V N-Channel MOSFET

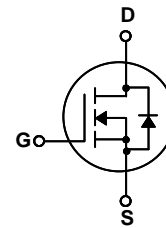
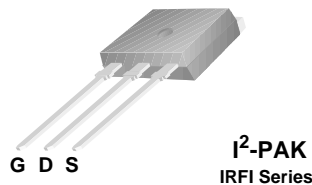
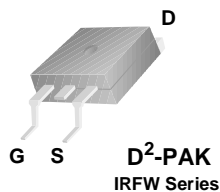
### General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switching DC/DC converter and switch mode power supplies.

### Features

- 14A, 250V,  $R_{DS(on)} = 0.28\Omega$  @  $V_{GS} = 10V$
- Low gate charge ( typical 47 nC)
- Low  $C_{rss}$  ( typical 30 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	IRFW644B / IRFI644B	Units
$V_{DSS}$	Drain-Source Voltage	250	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ )	14	A
	- Continuous ( $T_C = 100^\circ\text{C}$ )	8.9	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	56	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	480	mJ
$I_{AR}$	Avalanche Current (Note 1)	14	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	13.9	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ\text{C}$ ) *	3.13	W
	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	139	W
	- Derate above $25^\circ\text{C}$	1.11	W/ $^\circ\text{C}$
$T_J, T_{stg}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	0.9	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	40	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	$^\circ\text{C/W}$

\* When mounted on the minimum pad size recommended (PCB Mount)

**Electrical Characteristics** $T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	250	--	--	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.24	--	$V/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 250\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	$\mu\text{A}$
		$V_{DS} = 200\text{ V}, T_C = 125^\circ\text{C}$	--	--	100	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

**On Characteristics**

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 7.0\text{ A}$	--	0.22	0.28	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 7.0\text{ A}$ (Note 4)	--	11.7	--	S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	1250	1600	pF
$C_{oss}$	Output Capacitance		--	150	195	pF
$C_{rss}$	Reverse Transfer Capacitance		--	30	40	pF

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 125\text{ V}, I_D = 14\text{ A},$ $R_G = 25\text{ }\Omega$	--	20	50	ns
$t_r$	Turn-On Rise Time		--	115	240	ns
$t_{d(off)}$	Turn-Off Delay Time		--	150	310	ns
$t_f$	Turn-Off Fall Time	(Note 4, 5)	--	95	200	ns
$Q_g$	Total Gate Charge	$V_{DS} = 200\text{ V}, I_D = 14\text{ A},$ $V_{GS} = 10\text{ V}$	--	47	60	nC
$Q_{gs}$	Gate-Source Charge		--	6.2	--	nC
$Q_{gd}$	Gate-Drain Charge		--	23	--	nC

**Drain-Source Diode Characteristics and Maximum Ratings**

I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	14	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	56	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 14 A	--	--	1.5	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 14 A, dI <sub>F</sub> / dt = 100 A/μs (Note 4)	--	240	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	1.96	--	μC

**Notes:**

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 3.9\text{ mH}, I_{AS} = 14\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\text{ }\Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 14\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature

## Typical Characteristics

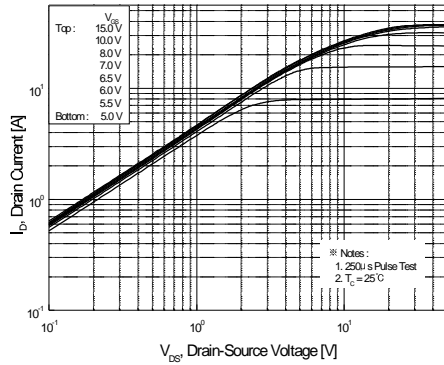


Figure 1. On-Region Characteristics

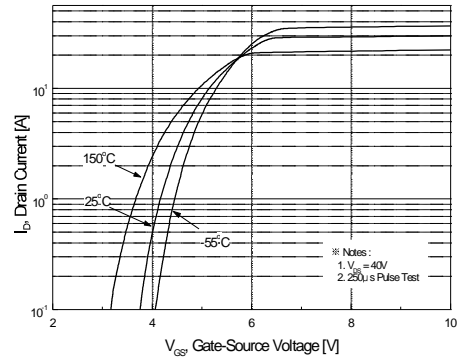


Figure 2. Transfer Characteristics

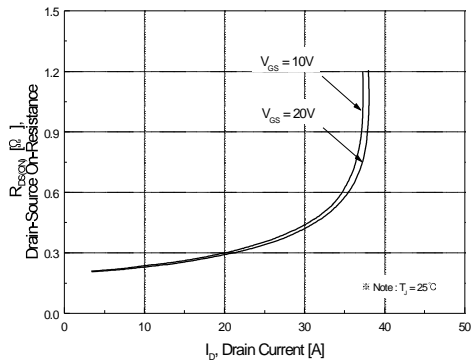


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

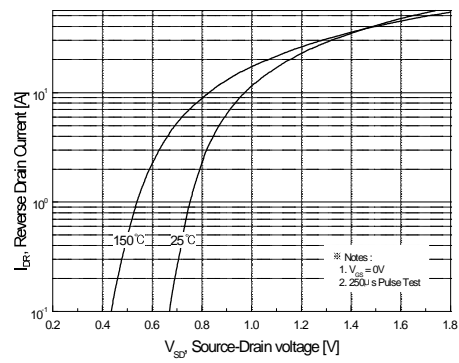


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

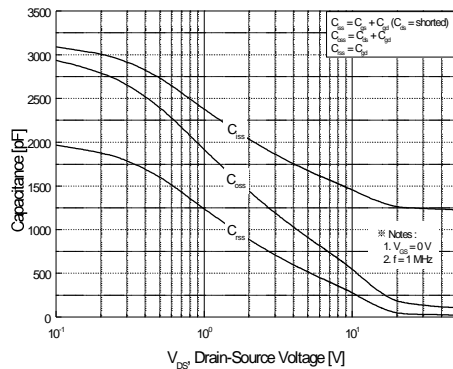


Figure 5. Capacitance Characteristics

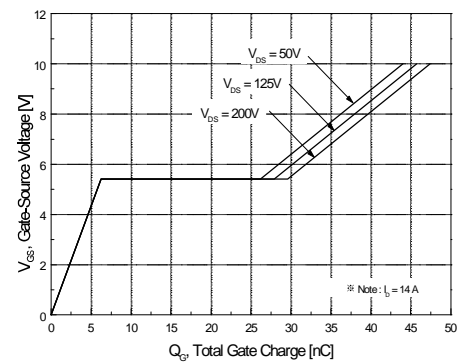
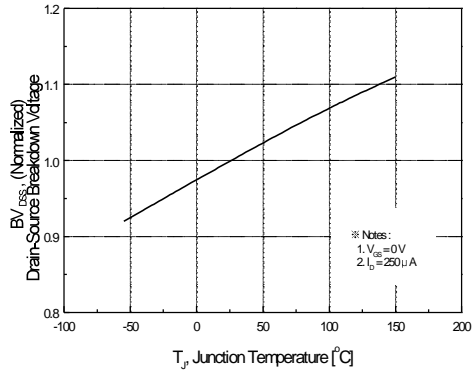
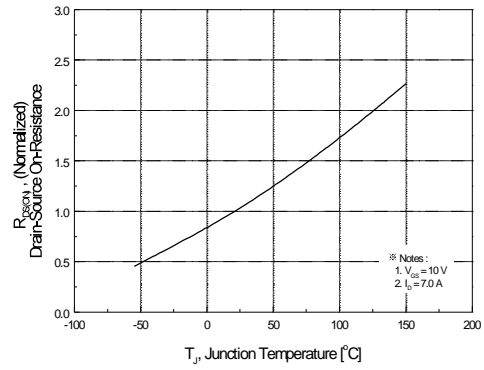


Figure 6. Gate Charge Characteristics

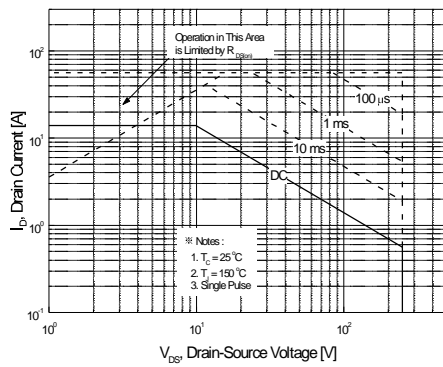
## Typical Characteristics (Continued)



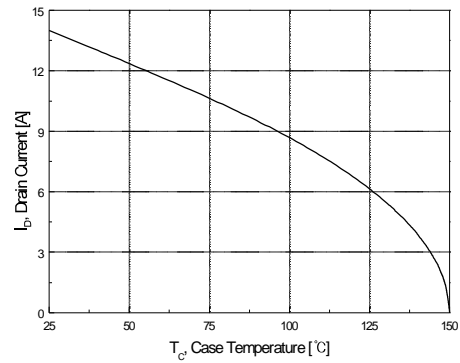
**Figure 7. Breakdown Voltage Variation vs Temperature**



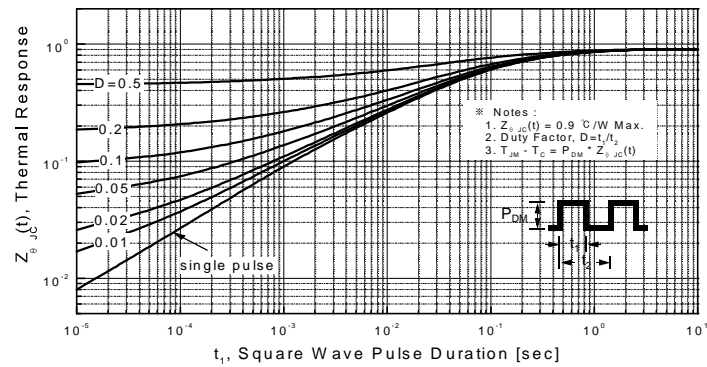
**Figure 8. On-Resistance Variation vs Temperature**



**Figure 9. Maximum Safe Operating Area**

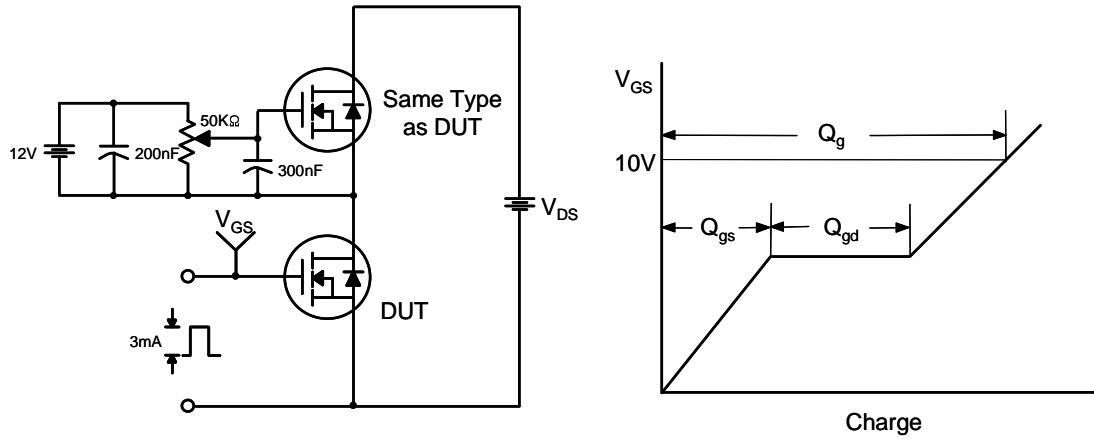


**Figure 10. Maximum Drain Current vs Case Temperature**

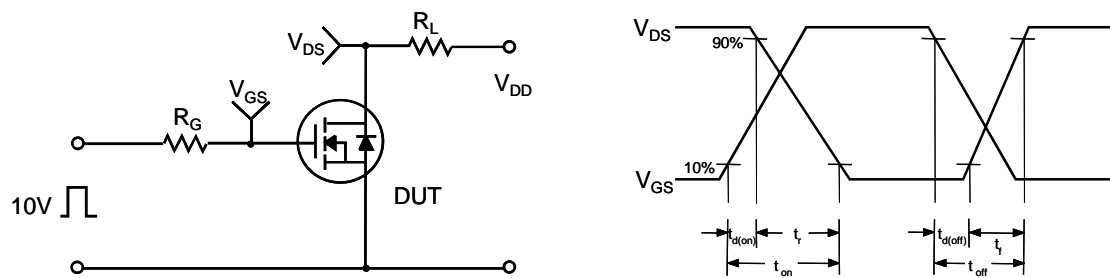


**Figure 11. Transient Thermal Response Curve**

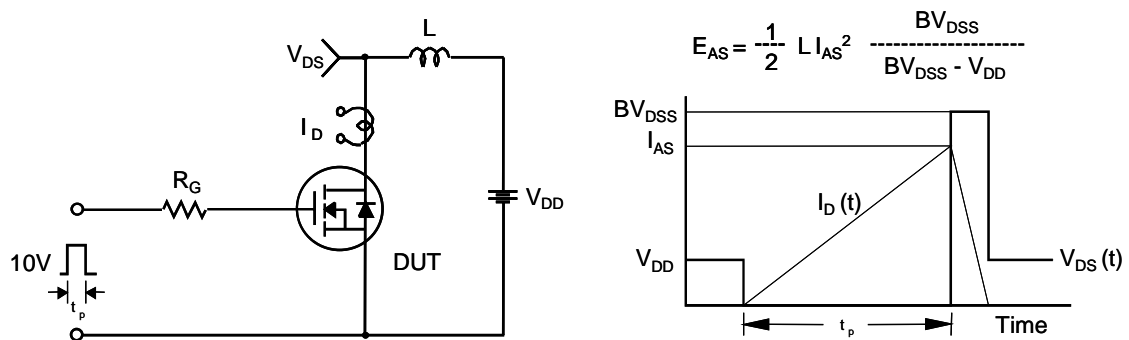
### Gate Charge Test Circuit & Waveform



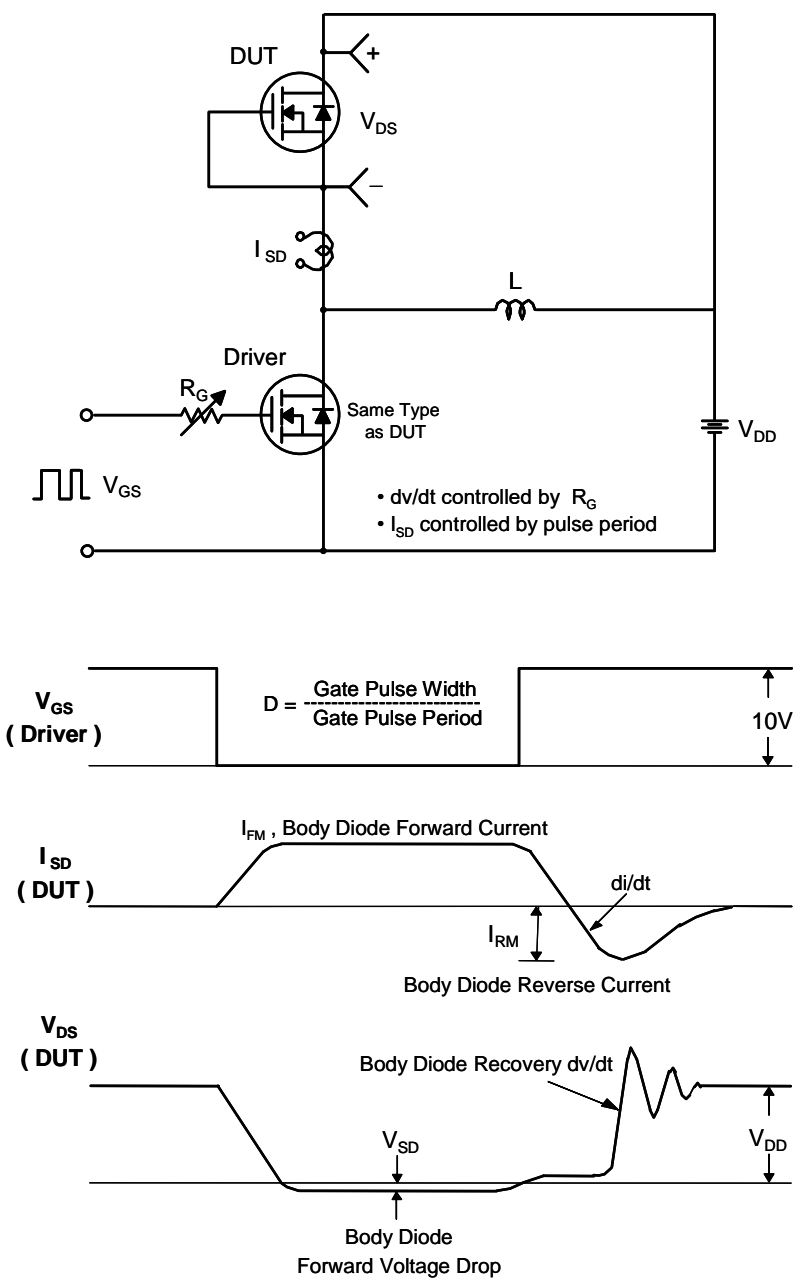
### Resistive Switching Test Circuit & Waveforms



### Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms



**IRFW644B / IRFI644B**

Technical drawing of a 10-pin D-sub connector, showing three views: front, side, and top. Dimensions are in millimeters (mm).

**Front View Dimensions:**

- Overall width:  $9.90 \pm 0.20$
- Overall height:  $15.30 \pm 0.30$
- Pin height (from base):  $4.90 \pm 0.20$
- Pin pitch:  $2.54$  TYP
- Pin diameter:  $0.80 \pm 0.10$
- Mounting hole diameter:  $1.27 \pm 0.10$
- Mounting hole pitch:  $2.54$  TYP
- Top flange thickness:  $1.40 \pm 0.20$
- Top flange outer diameter:  $(0.40)$
- Top flange inner diameter:  $1.20 \pm 0.20$
- Top flange hole diameter:  $9.20 \pm 0.20$

**Side View Dimensions:**

- Overall width:  $4.50 \pm 0.20$
- Overall height:  $2.54 \pm 0.30$
- Pin height (from base):  $2.00 \pm 0.10$
- Pin pitch:  $2.54$  TYP
- Pin diameter:  $0.80 \pm 0.10$
- Mounting hole diameter:  $1.27 \pm 0.10$
- Mounting hole pitch:  $2.54$  TYP
- Top flange thickness:  $1.40 \pm 0.20$
- Top flange outer diameter:  $(0.40)$
- Top flange inner diameter:  $1.20 \pm 0.20$
- Top flange hole diameter:  $9.20 \pm 0.20$

**Top View Dimensions:**

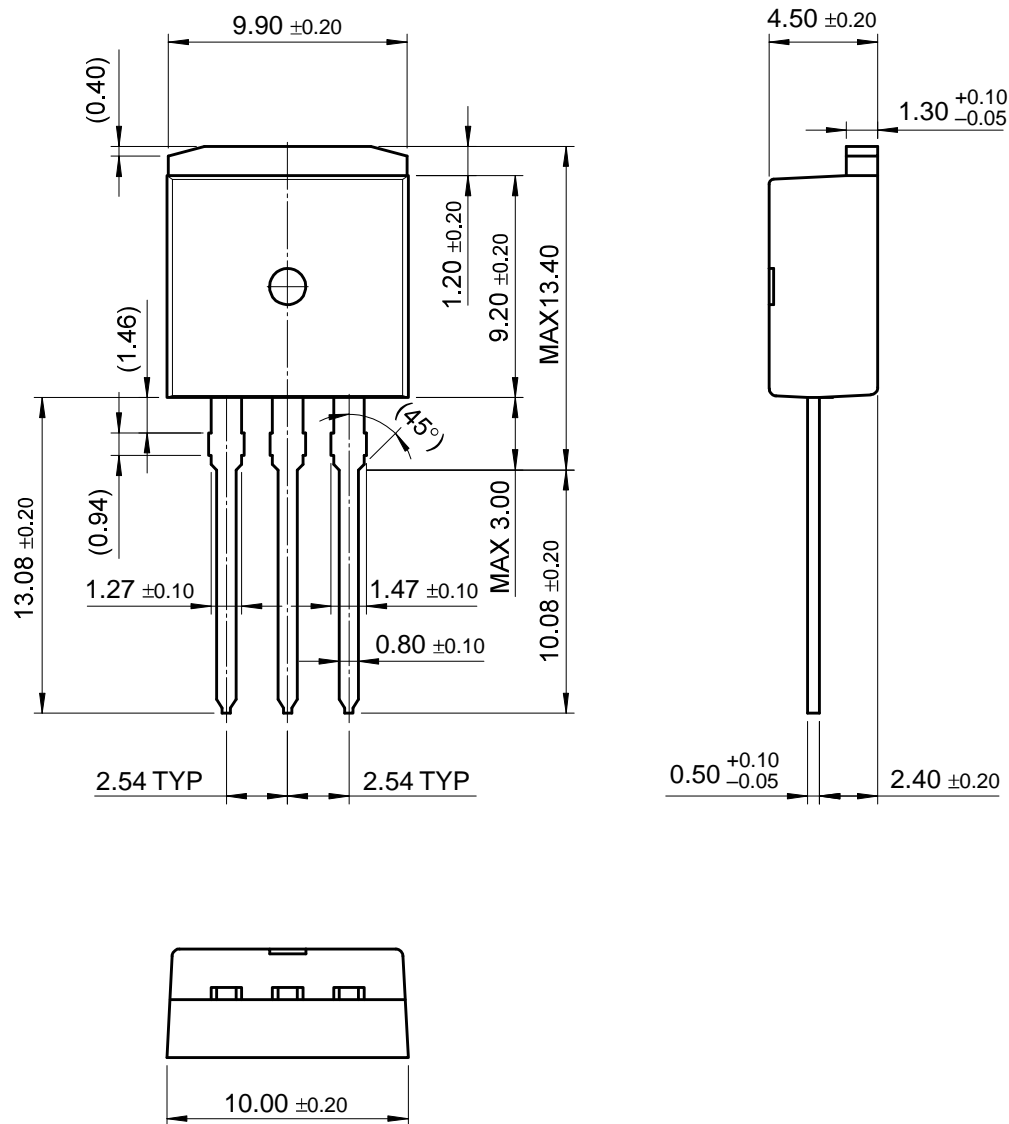
- Overall width:  $10.00 \pm 0.20$
- Overall height:  $9.20 \pm 0.20$
- Pin height (from base):  $4.90 \pm 0.20$
- Pin pitch:  $2.54$  TYP
- Pin diameter:  $0.80 \pm 0.10$
- Mounting hole diameter:  $1.27 \pm 0.10$
- Mounting hole pitch:  $2.54$  TYP
- Top flange thickness:  $1.40 \pm 0.20$
- Top flange outer diameter:  $(0.40)$
- Top flange inner diameter:  $1.20 \pm 0.20$
- Top flange hole diameter:  $9.20 \pm 0.20$

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Package Dimensions (Continued)

I<sup>2</sup>-PAK



Dimensions in Millimeters



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