

# The physical layer in the CAN FD world

With CAN FD data-rates can be raised up to 2 Mbit/s in multi-drop networks and up to 5 Mbit/s in point-to-point communication. Let's take a look at the impact that this development has on the physical layer.

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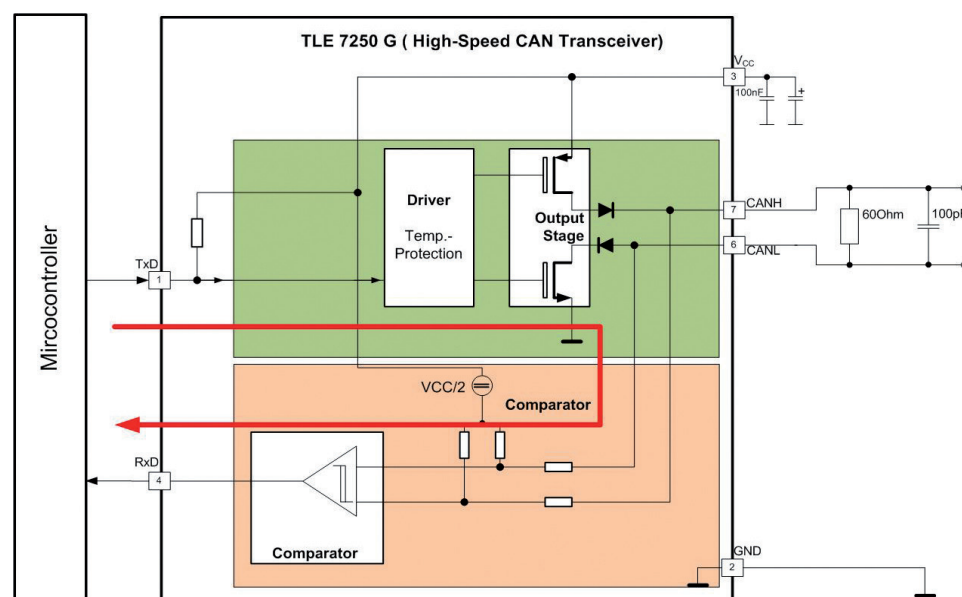


Figure 1: TxD-to-RxD transceiver propagation delay specification

In automotive applications CAN bit-rates of 125 kbit/s, 250 kbit/s, and 500 kbit/s are well approved. In the industrial area lower bit-rates down to 50 kbit/s and higher bit-rates up to 1 Mbit/s have been used for years. The ISO standards 11898-2, -5, and -6 are relevant for the development of so-called CAN high-speed transceivers. With the CAN FD protocol, the data-rate can be increased in the data-phase. At the moment, the automotive industry is discussing 2 Mbit/s in multi-drop networks and up to 5 Mbit/s in point-to-point communication. The impact on the physical layer, which includes the transceiver, the network, and the interface between microcontroller and transceiver, will be discussed in this article. In ISO 11898-2, -5, and -6, a lot of static parameters are specified, e.g.

the recessive and the dominant voltage level. But for higher bit-rates dynamic parameters are even more important. The only dynamic parameter for the physical layer is the TxD-to-RxD propagation delay (loop-delay) with a maximum value of 280 ns in the

current ISO 11898-2, and 255 ns in the current ISO 11898-5 standards. The ISO 11898-6 based on the ISO 11898-5 and the propagation delay specification is the same. This propagation delay is specified for the transceiver with a defined load, but in real applications ►

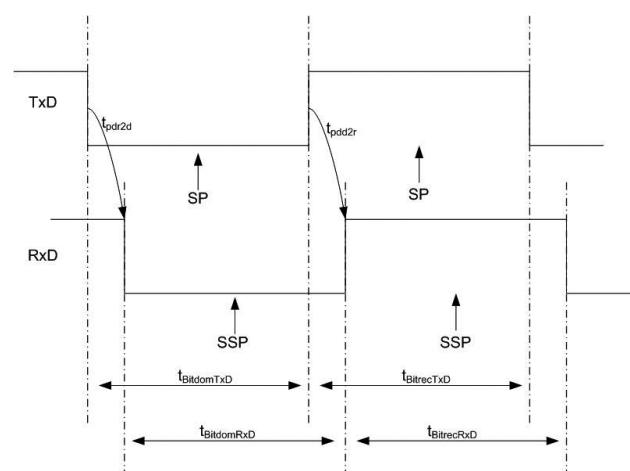


Figure 2: Transceiver with a perfect symmetric TxD-to-RxD propagation delay

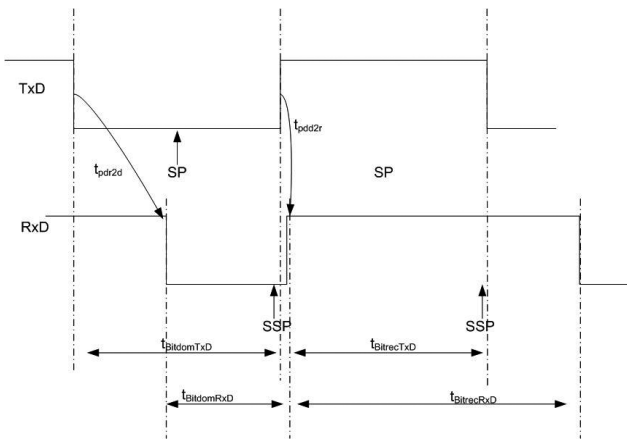


Figure 3: Transceiver with a very asymmetric TxD-to-RxD propagation delay

additional delays have to be taken into account, for example:

- ◆ Delay between micro-controller and transceiver;
- ◆ Delay of components improving the ESD and EMC robustness;
- ◆ Ringing, especially at the end of the dominant to recessive edge.

The TxD-to-RxD loop-delay is valid for the recessive-to-dominant transition and for the dominant-to-recessive transition.

The parameter is specified for a busload of 60  $\Omega$  and 100 pF. The disadvantage of this specification is that it allows a very asymmetric propagation delay for both transitions. This can shorten or expand the bit length of the recessive or dominant bits and limits the maximum possible bit-rate in the data phase of the CAN FD telegrams.

## Propagation delay symmetry

Figure 2 shows a very symmetric TxD-to-RxD propagation delay performance. The RxD bit-time of the dominant bits is the same as the bit-time of the TxD bits. In Figure 3 a very asymmetric behavior is shown. The dominant bit of RxD is extremely shortened and the recessive bit of RxD is expanded. Such an extreme asymmetry limits the minimum possible bit-time and the maximum

possible bit-rate. To optimize the transceiver behavior for CAN FD applications, the propagation delay symmetry needs to be specified. During analyses of several CAN transceivers on the market, we found out that the number of dominant bits in a row has an impact on the transceiver's behavior.

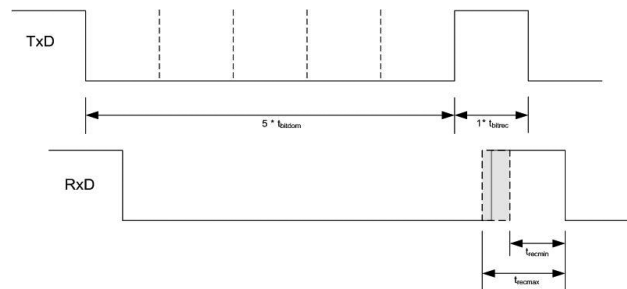


Figure 4: Propagation delay specification for CAN FD transceivers

To cover this observation in the specification, the bit-time of the recessive bit after five dominant bits in a row needs to be specified. Normally, lower bit-rates have no impact on this performance. This specification can be used for lower bit-rates, too. Two different bit-rates for the data-phase are in discussion at the moment: 2 Mbit/s for communication in complex networks and 5 Mbit/s for point-to-point communication. For higher bit-rates, a higher precision is needed. That is the reason why different limits are possible for 2 Mbit/s and for 5 Mbit/s. To cover this specification with one kind of transceiver the

temperature range and the 5-V supply ( $V_{CC}$ ) range are tailored.

The advantage of this proposal is that it can be used for lower bit-rates, too. This parameter shows that for all lower bit-rates the recessive bits will be shortened by up to 100 ns and can be expand by up to 50 ns. These values can now be used for the network design and the sample-point calculation in the arbitration-phase.

Another reason for asymmetric delay is the physical behavior of the network itself. CAN transceivers have open-drain output stages (see Figure 1) and no push-pull power stages like, for example, Flexray transceivers. This open-drain concept allows controlling the dominant level on the bus only and the recessive-to-dominant slew-rate to optimize

or EMC components, the dominant-to-recessive transition time can be increased and reduces the bit-time of a recessive bit. Figure 5 shows the impact of two different capacitive loads. In the upper part of Figure 5, the bus differential voltage behavior with a capacitive load of 220 pF is shown and on the bottom the same curve is shown for a capacitive load of 1,5 nF. Both edges have a smaller slew-rate, but the dominant bit is expanded. The length of the dominant bit-time depends on the threshold levels of the receiver like Figure 6 implies. A receiver with a high threshold (900 mV) detects a smaller dominant bit-time as a receiver with the minimum possible threshold.

## Further reasons for variation

Further reason for the asymmetry of the propagation delay is the temperature. Depending on the technology and the driver concept, the temperature coefficient can be positive or negative. Another reason for the variation of the asymmetry is the dominant differential voltage ( $V_{CAN\_H} - V_{CAN\_L}$ ) level. If the dominant voltage level is high, for example close to the maximum level of 3 V, the switch-off time becomes longer, until the differential voltage level is below the minimum receiver threshold level of 500 mV. The dominant differential voltage level depends on the fabrication variation of the Ron of CAN\_H and CAN\_L, the temperature, and the

Table 1: Specification for the TxD-to-RxD propagation delay symmetry

Recessive bit time	$t_{recmin}$	$t_{recmax}$
2 Mbit/sec $4,75 \text{ V} < V_{CC} < 5,25 \text{ V}$ $-40^\circ \text{C} \leq T_i \leq 150^\circ \text{C}$	400 ns	550 ns
5 Mbit/sec $4,85 \text{ V} < V_{CC} < 5,15 \text{ V}$ $-40^\circ \text{C} \leq T_i \leq 105^\circ \text{C}$	120 ns	220 ns

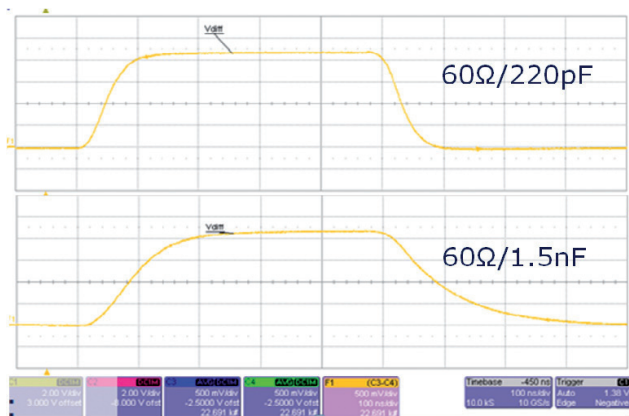


Figure 5: The impact of different capacitive load on the dominant bit-time

5-V power supply variation. For higher bit-rates the  $V_{CC}$  range and the temperature range are tightened to achieve a stable communication for higher bit-rates, too.

TxD output driver of the micro-controller and the slew-rate symmetry of the transceiver RxD output driver also has an impact on the symmetry. The capacitive load on the board as well as the capacitive input load

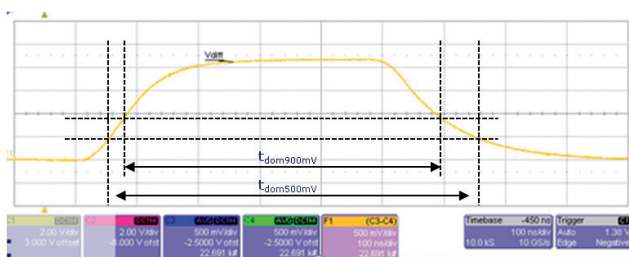


Figure 6: The maximum and minimum receiver threshold levels are marked

## MCU-to-transceiver interface

The interface between micro-controller and transceiver can also be a reason for asymmetric delay. The slew-rate symmetry of the

of the transceiver TxD input or the micro-controller RxD input can modify the symmetry. Especially, the input concept of the transceivers TxD input buffer like CMOS level input or TTL level input threshold can

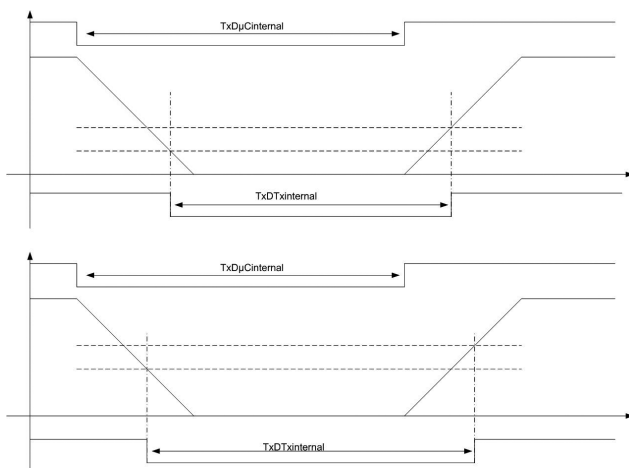


Figure 7: Comparison of TTL and CMOS transceiver TxD input concept

lead to additional asymmetry. The CMOS level input has less impact on the symmetry if the slew-rates of the output driver are perfectly matched. The asymmetry is dominated by the symmetry performance of the driver. If the transceiver TxD input has TTL input levels these thresholds add an additional asymmetry created by the thresholds itself.

Figure 7 shows an example with a very low input threshold and a very small hysteresis. The slew-rates of the driver are very symmetric, but the dominant bit-time is shortened by the TTL input stage. This asymmetry can be helpful, because it expands the recessive bit while normally the bus reduces the recessive bit-time. In point-to-point networks with a termination at both ends, this limits the bit-rate, too.

In Figure 8 the impact of asymmetric signals on the transceiver TxD input is shown. Asymmetric signals especially at high capacitive loads modify the bit-time of the recessive and dominant bits, as well. Therefore, the receiver and the micro-controller output drivers have to be symmetrical, especially for high capacitive loads.

In galvanically isolated applications with an optocoupler as interface between micro-controllers and transceiver, the propagation delay of the optocoupler

has to be taken into account. Optocoupler have an open drain output stage. The high-to-low edge (recessive to dominant) is driven by the output transistor. The dominant-to-recessive edge depends on the external RC circuitry.

Furthermore a reason for asymmetry is the ringing at the dominant-to-recessive transition. As a reminder: this is the uncontrolled transition. Terminated wires and star topologies are not the reason for ringing at this transition. Additionally, this ringing shortens the recessive bit. The recessive-to-dominant transition is less critical, because the transceiver controls this transition with its output stages. If a ringing is present it is damped by the powerful output stages.

## Sampling-point

Why is symmetry of the physical layer so important? The asymmetry of the physical layer reduces the possible range for the sampling-point. If we have a look at the latest possible sampling-point time then two different scenarios have to be checked. Scenario 1 is the maximum possible distance between two recessive to dominant edges, which can be synchronized again. That time is 10 bit-times. To calculate the latest possible sampling point the oscilla-

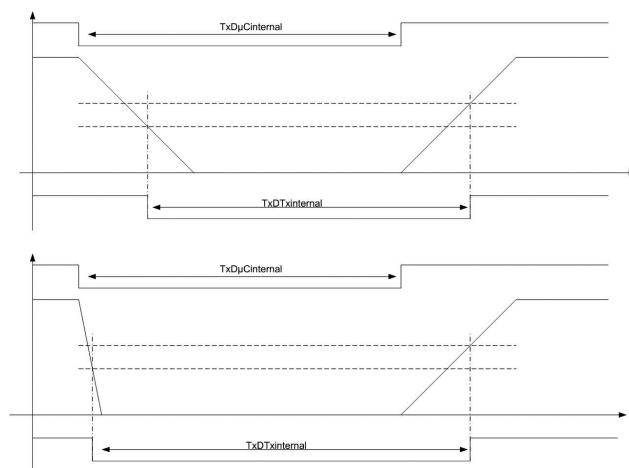


Figure 8: The impact of the transceiver internal bit-time depends on the slew rate

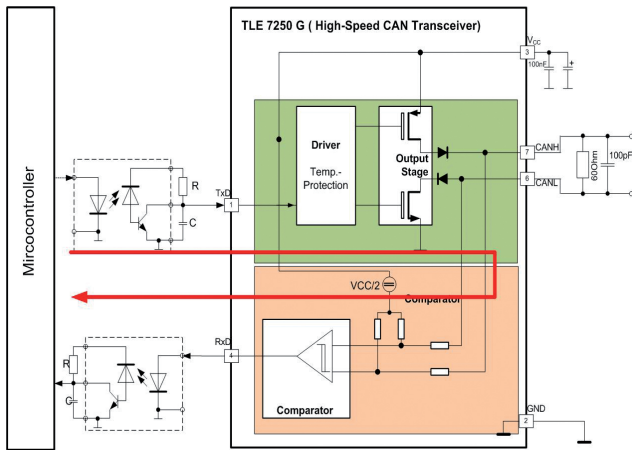


Figure 9: Optocoupler as an interface for isolation

tor tolerance of sender and receiver, the re-synchronization jump-width, and the asymmetry of the interface between micro-controller and transceiver have to be taken into account.

Scenario 2 is the 5-bit case with the maximum number of dominant bits in a row. In this scenario, the above-mentioned points have to be considered as well as the transceiver asymmetry (50 ns for 2 Mbit/s and 20 ns for 5 Mbit/s). For the earliest possible sampling-time, the recessive bit after five dominant bits is the most critical situation. In this scenario, the transceiver asymmetry (100 ns for 2 Mbit/s or 80 ns for 5 Mbit/s), the network ringing, and the bus-load have to be taken into account, besides the other points.

To get a successful and stable communication in a CAN FD network running at higher bit-rates (2 Mbit/s and more), special CAN FD transceivers should be used. Additionally, it is recommended to use a linear network topology with short stubs. The capacitive bus-load should be low as well as the capacitive loads on the ECU board. An intensive analysis of the sampling-point is necessary. The new parameter for transceivers will be helpful for classical CAN networks and for CAN FD networks. For classical CAN networks, these parameters help calculate

the sampling-point more easily or more reliable. No values must be evaluated or estimated by the user, because they will be given in future datasheets. Standardization will start at the beginning of 2014. The ISO 11898-2, -5, and -6 parts will be harmonized and the new parameter will be added. Infineon will start the investigation on existing CAN transceivers and add this new parameter to the datasheets. ◀

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